REMARKS

The Examiner is thanked for the thorough examination and search of the subject.

Claims 281-370 are pending; Claims 281-299, 301-312, 314-328, 330-343, 345-355, 357-367, 369 and 370 have been currently amended; Claims 1-280 have been canceled.

Response to Claim Rejections under 35 U.S.C. 102 and 103

Applicants respectfully traverse the rejections for at least the reasons set forth below.

Response to Claims 281 and 287-300

As currently amended, independent Claim 281 is recited below:

281. A method for fabricating a chip package, comprising:

joining a first side of a die and a substrate using an adhesive material;

after said joining said first side of said die and said substrate, forming a first polymer layer over a second side of said die, over said substrate and across an edge of said die, wherein said first and second sides are opposite to each other;

after said forming said first polymer layer, forming a circuit layer on said first polymer layer, over said second side of said die, over said substrate and across said edge of said die, wherein said forming said circuit layer comprises a copper electroplating process;

after said forming said circuit layer, forming an insulating layer on said circuit layer, on said first polymer layer, over said second side of said die, over said

substrate and across said edge of said die;

after said forming said circuit layer, forming a gold bump over said circuit layer; and

after said forming said gold bump over said circuit layer, cutting said substrate.

Reconsiderations of Claims 281, 287-300 rejected under 35 U.S.C. 103(a) as being unpatentable over Eichelberger et al. (U.S. Pat. No. 6,396,148) in view of Kim et al. (U.S. Pat. No. 6,004,867) are requested based on the following remarks.

Applicants respectfully assert that the method as claimed in Claim 281 patentably distinguishes over the citations by Eichelberger et al. (U.S. Pat. No. 6,396,148) in view of Kim et al. (U.S. Pat. No. 6,004,867).

The Examiner considers that "Gold, however, is a known material and commonly used in semiconductor art for forming bumps as disclosed by Kim (col. 6, lines 59+). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to select gold for forming bumps in "Eic-148" chip package since gold bumps is commonly used in semiconductor art, as disclosed by Kim. Motivation to do so would have improved the electrical connection and prevented the oxidization of the bumps". ~ *See lines 9-14 on page 3, in the last Office Action mailed Nov. 30, 2007* ~

The applicants respectfully traverse the Examiner's opinion because it would have been not obvious to a person of ordinary skill in the art at the time the invention was made to select gold for forming bumps in Eichelberger et al.'s chip package. Eichelberger et al. teach that multiple solder balls are formed over a substrate, which is not believed to be a wafer, joined with multiple dies using an adhesive material. Kim et

al. teach how multiple gold bumps are formed over a wafer; but fail to teach multiple gold bumps may be formed over a substrate joined with multiple dies using an adhesive material. It is believed that the gold bumps in Kim et al.'s device is non-analogous to solder balls in Eichelberger et al.'s device because the place having multiple gold bumps formed thereon, in Kim et al.'s device, is different from the place having multiple solder balls formed thereon, in Eichelberger et al.'s device.

Furthermore, both Eichelberger et al. and Kim et al. fail to teach, hint or suggest that a circuit layer on a polymer layer, over a die, over a substrate and across an edge of the die may be formed by a process comprising a copper electroplating process, as currently claimed in Claim 281.

Withdrawal of rejection under 35 U.S.C. 103(a) to Claim 281 is respectfully requested.

For at least the foregoing reasons, applicants respectfully submit independent Claim 281 patently distinguishes over the prior art references, and should be allowed. For at least the same reasons, dependent Claims 287-300 patently define over the prior art as well.

Response to Claims 282 and 301-319

As currently amended, independent Claim 282 is recited below:

282. A method for fabricating a chip package, comprising:

joining a first side of a die and a substrate using an adhesive material;

after said joining said first side of said die and said substrate, forming a first polymer layer over a second side of said die, over said substrate and across an edge

of said die, wherein said first and second sides are opposite to each other;

after said forming said first polymer layer, forming a circuit layer on said first polymer layer, over said second side of said die, over said substrate and across said edge of said die, wherein said forming said circuit layer comprises a copper electroplating process, and wherein said circuit layer comprises a portion acting as a part of an inductor;

after said forming said circuit layer, forming a second polymer layer on said circuit layer, on said first polymer layer, over said second side of said die, over said substrate and across said edge of said die;

after said forming said second polymer layer, forming a metal bump over said substrate, wherein said metal bump is connected to said die through said circuit layer; and

after said forming said metal bump, cutting said substrate.

Reconsiderations of Claims 282, 301-316 and 318 rejected under 35 U.S.C. 103(a) as being unpatentable over Eichelberger et al. (U.S. Pat. No. 6,396,148) in view of Wojnarowski et al. (U.S. Pat. No. 5,576,517), of Claim 317 rejected under 35 U.S.C. 103(a) as being unpatentable over Eichelberger et al. in view of Wojnarowski et al. (U.S. Pat. No. 5,576,517) further in view of Saia et al. (U.S. Pat. No. 5,874,770) and of Claim 319 rejected under 35 U.S.C. 103(a) as being unpatentable over Eichelberger et al. in view of Wojnarowski et al. (U.S. Pat. No. 5,576,517) further in view of Kim et al. (U.S. Pat. No. 6,004,867) are requested based on the following remarks.

Applicants respectfully assert that the method as claimed in Claim 282 patentably distinguishes over the citations by Eichelberger et al. (U.S. Pat. No. 6,396,148) in view of Wojnarowski et al. (U.S. Pat. No. 5,576,517).

Both Eichelberger et al. and Wojnarowski et al. fail to teach, hint or suggest that a circuit layer formed on a polymer layer, over a die, over a substrate and across an edge of the die may comprise a portion acting as a part of an inductor, as currently claimed in Claim 282.

Furthermore, both Eichelberger et al. and Wojnarowski et al. fail to teach, hint or suggest that a circuit layer on a polymer layer, over a die, over a substrate and across an edge of the die may be formed by a process comprising a copper electroplating process, as currently claimed in Claim 282.

Withdrawal of rejection under 35 U.S.C. 103(a) to Claim 282 is respectfully requested.

For at least the foregoing reasons, applicants respectfully submit independent Claim 282 patently distinguishes over the prior art references, and should be allowed. For at least the same reasons, dependent Claims 301-319 patently define over the prior art as well.

Response to Claims 283 and 320-334

As currently amended, independent Claim 283 is recited below:

283. A method for fabricating a chip package, comprising:

joining a first side of a die and a substrate using an adhesive material;

after said joining said first side of said die and said substrate, forming a first polymer layer over a second side of said die, over said substrate and across an edge of said die, wherein said first and second sides are opposite to each other;

after said forming said first polymer layer, forming a circuit layer on said

first polymer layer, over said second side of said die, over said substrate and across said edge of said die, wherein said forming said circuit layer comprises a copper electroplating process, and wherein said circuit layer comprises a portion acting as a part of a resistor;

after said forming said circuit layer, forming a second polymer layer on said circuit layer, on said first polymer layer, over said second side of said die, over said substrate and across said edge of said die;

after said forming said second polymer layer, forming a metal bump over said substrate, wherein said metal bump is connected to said die through said circuit layer; and

after said forming said metal bump, cutting said substrate.

Reconsiderations of Claims 283 and 320-334 rejected under 35 U.S.C. 103(a) as being unpatentable over Eichelberger et al. (U.S. Pat. No. 6,396,148) in view of Kim et al. (U.S. Pat. No. 6,004,867) further in view of Saia et al. (U.S. Pat. No. 5,874,770) are requested based on the following remarks.

Applicants respectfully assert that the method as claimed in Claim 283 patentably distinguishes over the citations by Eichelberger et al. (U.S. Pat. No. 6,396,148) in view of Kim et al. (U.S. Pat. No. 6,004,867) further in view of Saia et al. (U.S. Pat. No. 5,874,770).

The Examiner considers that "Saia while related to a similar method of fabricating a chip package teaches (see specifically figures 1-12) passive devices, including resistor, capacitor, inductor, etc., can be fabricated on both surface of the dielectric formed on the die (See Abstract). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to apply Saia method to the proposed chip package of

"Eic-148" and Kim in order to have passive devices being fabricated on the dielectric formed on the die and such application is held to be within the ordinary designing ability expected of a person skilled in the art". *-- See lines 9-16 on page 6, in the last Office Action mailed Nov. 30, 2007 --*

The applicants respectfully traverse the Examiner's opinion because it would have been not obvious to a person of ordinary skill in the art at the time the invention was made to apply Saia method to Eichelberger et al.'s chip package. Eichelberger et al. teach multiple circuit layers are formed over a substrate and over a die after the die is joined with the substrate. Saia et al. teach that a circuit layer having a portion serving as a passive device are formed before a die is joined with a substrate having the passive device, but fail to teach, hint or suggest that a circuit layer having a portion serving as a passive device may be formed over a die and over a substrate after the die is joined with the substrate. It is believed that the circuit layer having a portion serving as a passive device, in Saia et al.'s device, is non-analogous to the circuit layer in Eichelberger et al.'s device because the order of forming the circuit layer having a portion serving as a passive device, in Saia et al.'s device, and joining a die with a substrate having the passive device, is contrary to the order of forming the circuit layer, in Eichelberger et al.'s device, and joining a die with a substrate. No one teaches a circuit layer comprising a portion acting as a part of a resistor can be formed over a die, over a substrate and across an edge of the die after the die is joined with the substrate, as currently claimed in Claim 283.

Withdrawal of rejection under 35 U.S.C. 103(a) to Claim 283 is respectfully requested.

For at least the foregoing reasons, applicants respectfully submit independent Claim 283 patently distinguishes over the prior art references, and should be allowed. For at least the same reasons, dependent Claims 320-334 patently define over the prior art

as well.

Response to Claims 284 and 335-346

As currently amended, independent Claim 284 is recited below:

284. A method for fabricating a chip package, comprising:

joining a first side of a die and a substrate using an adhesive material;

after said joining said first side of said die and said substrate, forming a first polymer layer over a second side of said die, over said substrate and across an edge of said die, wherein said first and second sides are opposite to each other;

after said forming said first polymer layer, forming a circuit layer on said first polymer layer, over said second side of said die, over said substrate and across said edge of said die, wherein said forming said circuit layer comprises a copper electroplating process, and wherein said circuit layer comprises a portion acting as a part of a waveguide;

after said forming said circuit layer, forming a second polymer layer on said circuit layer, on said first polymer layer, over said second side of said die, over said substrate and across said edge of said die;

after said forming said second polymer layer, forming a metal bump over said substrate, wherein said metal bump is connected to said die through said circuit layer; and

after said forming said metal bump, cutting said substrate.

Reconsiderations of Claims 284 and 335-346 rejected under 35 U.S.C. 103(a) as being unpatentable over Eichelberger et al. (U.S. Pat. No. 6,396,148) in view of Kim et al. (U.S. Pat. No. 6,004,867) further in view of Saia et al. (U.S. Pat. No. 5,874,770) are

requested based on the following remarks.

Applicants respectfully assert that the method as claimed in Claim 284 patentably distinguishes over the citations by Eichelberger et al. (U.S. Pat. No. 6,396,148) in view of Kim et al. (U.S. Pat. No. 6,004,867) further in view of Saia et al. (U.S. Pat. No. 5,874,770).

The Examiner considers that "Saia while related to a similar method of fabricating a chip package teaches (see specifically figures 1-12) passive devices, including resistor, capacitor, inductor, etc., can be fabricated on both surface of the dielectric formed on the die (See Abstract). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to apply Saia method to the proposed chip package of "Eic-148" and Kim in order to have passive devices being fabricated on the dielectric formed on the die and such application is held to be within the ordinary designing ability expected of a person skilled in the art". *~ See lines 9-16 on page 6, in the last Office Action mailed Nov. 30, 2007 ~*

The applicants respectfully traverse the Examiner's opinion because it would have been not obvious to a person of ordinary skill in the art at the time the invention was made to apply Saia method to Eichelberger et al.'s chip package. Eichelberger et al. teach multiple circuit layers are formed over a substrate and over a die after the die is joined with the substrate. Saia et al. teach that a circuit layer having a portion serving as a passive device are formed before a die is joined with a substrate having the passive device, but fail to teach, hint or suggest that a circuit layer having a portion serving as a passive device may be formed over a die and over a substrate after the die is joined with the substrate. It is believed that the circuit layer having a portion serving as a passive device, in Saia et al.'s device, is non-analogous to the circuit layer in Eichelberger et al.'s device because the order of forming the circuit layer having a portion serving as a passive

device, in Saia et al.'s device, and joining a die with a substrate having the passive device, is contrary to the order of forming the circuit layer, in Eichelberger et al.'s device, and joining a die with a substrate. No one teaches a circuit layer comprising a portion acting as a part of a waveguide can be formed over a die, over a substrate and across an edge of the die after the die is joined with the substrate, as currently claimed in Claim 284.

The Examiner considers that "the selection of other passive device (e.g., a waveguide in claims 284 and 335-346; a micro electronic mechanical element in claims 285 and 347-358; and a filter in claims 286 and 359-370) to be formed on the chip package would have been obvious for similar reasons set forth above". ~ *See lines 17-20 on page 6, in the last Office Action mailed Nov. 30, 2007* ~

The applicants respectfully traverse the Examiner's opinion because both Eichelberger et al. and Saia et al. fail to teach a circuit layer comprising a portion acting as a part of a waveguide can be formed over a die, over a substrate and across an edge of the die after the die is joined with the substrate, as currently claimed in Claim 284.

Withdrawal of rejection under 35 U.S.C. 103(a) to Claim 284 is respectfully requested.

For at least the foregoing reasons, applicants respectfully submit independent Claim 284 patently distinguishes over the prior art references, and should be allowed. For at least the same reasons, dependent Claims 335-346 patently define over the prior art as well.

Response to Claims 285 and 347-358

As currently amended, independent Claim 285 is recited below:

285. A method for fabricating a chip package, comprising:

joining a first side of a die and a substrate using an adhesive material;

after said joining said first side of said die and said substrate, forming a first polymer layer over a second side of said die, over said substrate and across an edge of said die, wherein said first and second sides are opposite to each other;

after said forming said first polymer layer, forming a circuit layer on said first polymer layer, over said second side of said die, over said substrate and across said edge of said die, wherein said forming said circuit layer comprises a copper electroplating process, and wherein said circuit layer comprises a portion acting as a part of a capacitor;

after said forming said circuit layer, forming a second polymer layer on said circuit layer, on said first polymer layer, over said second side of said die, over said substrate and across said edge of said die;

after said forming said second polymer layer, forming a metal bump over said substrate, wherein said metal bump is connected to said die through said circuit layer; and

after said forming said metal bump, cutting said substrate.

Reconsiderations of Claims 285 and 347-358 rejected under 35 U.S.C. 103(a) as being unpatentable over Eichelberger et al. (U.S. Pat. No. 6,396,148) in view of Kim et al. (U.S. Pat. No. 6,004,867) further in view of Saia et al. (U.S. Pat. No. 5,874,770) are requested based on the following remarks.

Applicants respectfully assert that the method as claimed in Claim 285 patentably distinguishes over the citations by Eichelberger et al. (U.S. Pat. No. 6,396,148) in view of Kim et al. (U.S. Pat. No. 6,004,867) further in view of Saia et al. (U.S. Pat. No.

5,874,770).

The Examiner considers that "Saia while related to a similar method of fabricating a chip package teaches (see specifically figures 1-12) passive devices, including resistor, capacitor, inductor, etc., can be fabricated on both surface of the dielectric formed on the die (See Abstract). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to apply Saia method to the proposed chip package of "Eic-148" and Kim in order to have passive devices being fabricated on the dielectric formed on the die and such application is held to be within the ordinary designing ability expected of a person skilled in the art". *~ See lines 9-16 on page 6, in the last Office Action mailed Nov. 30, 2007 ~*

The applicants respectfully traverse the Examiner's opinion because it would have been not obvious to a person of ordinary skill in the art at the time the invention was made to apply Saia method to Eichelberger et al.'s chip package. Eichelberger et al. teach multiple circuit layers are formed over a substrate and over a die after the die is joined with the substrate. Saia et al. teach that a circuit layer having a portion serving as a passive device are formed before a die is joined with a substrate having the passive device, but fail to teach, hint or suggest that a circuit layer having a portion serving as a passive device may be formed over a die and over a substrate after the die is joined with the substrate. It is believed that the circuit layer having a portion serving as a passive device, in Saia et al.'s device, is non-analogous to the circuit layer in Eichelberger et al.'s device because the order of forming the circuit layer having a portion serving as a passive device, in Saia et al.'s device, and joining a die with a substrate having the passive device, is contrary to the order of forming the circuit layer, in Eichelberger et al.'s device, and joining a die with a substrate. No one teaches a circuit layer comprising a portion acting as a part of a capacitor can be formed over a die, over a substrate and across an edge of the die after the die is joined with the substrate, as currently claimed in Claim 285.

Withdrawal of rejection under 35 U.S.C. 103(a) to Claim 285 is respectfully requested.

For at least the foregoing reasons, applicants respectfully submit independent Claim 285 patently distinguishes over the prior art references, and should be allowed. For at least the same reasons, dependent Claims 347-358 patently define over the prior art as well.

Response to Claims 286 and 359-370

As currently amended, independent Claim 286 is recited below:

286. A method for fabricating a chip package, comprising:

joining a first side of a die and a substrate using an adhesive material;

after said joining said first side of said die and said substrate, forming a first polymer layer over a second side of said die, over said substrate and across an edge of said die, wherein said first and second sides are opposite to each other;

after said forming said first polymer layer, forming a circuit layer on said first polymer layer, over said second side of said die, over said substrate and across said edge of said die, wherein said forming said circuit layer comprises a copper electroplating process, and wherein said circuit layer comprises a portion acting as a part of a filter;

after said forming said circuit layer, forming a second polymer layer on said circuit layer, on said first polymer layer, over said second side of said die, over said substrate and across said edge of said die;

after said forming said second polymer layer, forming a metal bump over said substrate, wherein said metal bump is connected to said die through said circuit

layer; and

after said forming said metal bump, cutting said substrate.

Reconsiderations of Claims 286 and 359-370 rejected under 35 U.S.C. 103(a) as being unpatentable over Eichelberger et al. (U.S. Pat. No. 6,396,148) in view of Kim et al. (U.S. Pat. No. 6,004,867) further in view of Saia et al. (U.S. Pat. No. 5,874,770) are requested based on the following remarks.

Applicants respectfully assert that the method as claimed in Claim 286 patentably distinguishes over the citations by Eichelberger et al. (U.S. Pat. No. 6,396,148) in view of Kim et al. (U.S. Pat. No. 6,004,867) further in view of Saia et al. (U.S. Pat. No. 5,874,770).

The Examiner considers that "Saia while related to a similar method of fabricating a chip package teaches (see specifically figures 1-12) passive devices, including resistor, capacitor, inductor, etc., can be fabricated on both surface of the dielectric formed on the die (See Abstract). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to apply Saia method to the proposed chip package of "Eic-148" and Kim in order to have passive devices being fabricated on the dielectric formed on the die and such application is held to be within the ordinary designing ability expected of a person skilled in the art". *~ See lines 9-16 on page 6, in the last Office Action mailed Nov. 30, 2007 ~*

The applicants respectfully traverse the Examiner's opinion because it would have been not obvious to a person of ordinary skill in the art at the time the invention was made to apply Saia method to Eichelberger et al.'s chip package. Eichelberger et al. teach multiple circuit layers are formed over a substrate and over a die after the die is

joined with the substrate. Saia et al. teach that a circuit layer having a portion serving as a passive device are formed before a die is joined with a substrate having the passive device, but fail to teach, hint or suggest that a circuit layer having a portion serving as a passive device may be formed over a die and over a substrate after the die is joined with the substrate. It is believed that the circuit layer having a portion serving as a passive device, in Saia et al.'s device, is non-analogous to the circuit layer in Eichelberger et al.'s device because the order of forming the circuit layer having a portion serving as a passive device, in Saia et al.'s device, and joining a die with a substrate having the passive device, is contrary to the order of forming the circuit layer, in Eichelberger et al.'s device, and joining a die with a substrate. No one teaches a circuit layer comprising a portion acting as a part of a filter can be formed over a die, over a substrate and across an edge of the die after the die is joined with the substrate, as currently claimed in Claim 284.

The Examiner considers that "the selection of other passive device (e.g., a waveguide in claims 284 and 335-346; a micro electronic mechanical element in claims 285 and 347-358; and a filter in claims 286 and 359-370) to be formed on the chip package would have been obvious for similar reasons set forth above". ~ *See lines 17-20 on page 6, in the last Office Action mailed Nov. 30, 2007* ~

The applicants respectfully traverse the Examiner's opinion because both Eichelberger et al. and Saia et al. fail to teach a circuit layer comprising a portion acting as a part of a filter can be formed over a die, over a substrate and across an edge of the die after the die is joined with the substrate, as currently claimed in Claim 286.

Withdrawal of rejection under 35 U.S.C. 103(a) to Claim 286 is respectfully requested.

For at least the foregoing reasons, applicants respectfully submit independent

Claim 286 patently distinguishes over the prior art references, and should be allowed. For at least the same reasons, dependent Claims 359-370 patently define over the prior art as well.

CONCLUSION

Some or all of the pending claims are believed to be in condition for Allowance, and that is so requested. Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Sincerely yours,

/ Winston Hsu / Date: 02.29.2008

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Note: Please leave a message in my voice mail if you need to talk to me. (The time in D.C. is 13 hours behind the Taiwan time, i.e. 9 AM in D.C. = 10 PM in Taiwan.)